What is Claimed is:

1. A field effect transistor formed in a semiconductor layer which has a strain effect and which is formed in an upper layer of a semiconductor substrate, said field effect transistor comprising:

a source/a drain formed only in said semiconductor layer having the strain effect.

2. A field effect transistor according to claim 1, wherein said semiconductor layer having the strain effect comprises a silicon layer having a strain effect.

3. A field effect transistor according to claim 2, further comprising:

silicon epitaxial layers formed on said sourc e/drain; and refractory metal silicide layers formed on said silicon epitaxial layers.

4. A field effect transistor according to claim 2, wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress

is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

5. A field effect transistor according to claim 3, wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

6. A method of fabricating a field effect transistor, comprising the steps of:

forming a semiconductor substrate in such a manner that a semiconductor layer having a strain effect is formed in an upper layer of said semiconductor substrate;

forming a gate electrode on said semiconductor layer having the strain effect through a gate insulating film; and

forming a source/a drain by doping an impurity for

forming the source/drain in said semiconductor layer having the strain effect on both sides of said gate electrode.

7. A method of fabricating a field effect transistor according to claim 6, wherein said semiconductor layer having the strain effect comprises a silicon layer having a strain effect.

8. A method of fabricating a field effect transistor according to claim 7, further comprising the steps of:

forming, after formation of said source/drain, silicon epitaxial layers on said source/drain; and

forming refractory metal silicide layers on said silicon epitaxial layers.

9. A semiconductor device comprising:

a p-channel type field effect transistor and an n-channel type field effect transistor both formed in a semiconductor layer which has a strain effect and which is formed in an upper layer of a semiconductor substrate,

wherein a source/a drain of said p-channel type field effect transistor and a source/a drain of said n-channel type field effect transistor are formed only in said semiconductor layer having the strain effect.

10. A semiconductor device according to claim 9, wherein said semiconductor layer having the strain effect

comprises a silicon layer having a strain effect.

11. A semiconductor device according to claim 10, wherein each of said p-channel type field effect transistor and said n-channel type field effect transistor comprises:

silicon epitaxial layers formed on said sourc e/drain; and

refractory metal silicide layers formed on said silicon epitaxial layers.

12. A semiconductor device according to claim 10, wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

13. A semiconductor device according to claim 11, wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said

buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

14. A method of fabricating a semiconductor device, comprising the steps of:

forming a semiconductor substrate in such a manner that a silicon layer having a strain effect is formed in an upper layer of said semiconductor substrate;

forming a gate electrode of a p-channel type field effect transistor and a gate electrode of a n-channel type field effect transistor on said silicon layer having the strain effect through a gate insulating film;

forming a source/a drain composed of p-type diffusion layers in said silicon layer having the strain effect on both sides of said gate electrode of said p-channel type field effect transistor; and

forming a source/a drain composed of n-type diffusion layers in said silicon layer having the strain effect on both sides of said gate electrode of said n-

channel type field effect transistor.

15. A method of fabricating a semiconductor device according to claim 14, further comprising the steps of:

forming, after formation of each source/drain, silicon epitaxial layers on said source/drain; and

forming refractory metal silicide layers on said silicon epitaxial layers.

16. A logic circuit comprising:

a semiconductor device having a p-channel type field effect transistor and an n-channel type field effect transistor;

wherein a semiconductor substrate on which said logic circuit is formed comprises a semiconductor substrate in which a silicon layer having a strain effect is formed in an upper layer thereof;

a source/a drain of said p-channel type field effect transistor are formed only in said silicon layer having the strain effect; and

a source/a drain of said n-channel type field effect transistor are formed only in said silicon layer having the strain effect.

17. A semiconductor substrate comprising:

a germanium base;

a relax layer formed on said germanium base, said

relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

18. A field effect transistor according to claim 2, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

19. A field effect transistor according to claim 3, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

20. A semiconductor device according to claim 10, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said

relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

21. A semiconductor device according to claim 11, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.